SALICIDE PROCESS FOR METAL GATE CMOS DEVICES

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to a method of forming self-aligned metal silicide (SALICDE) regions for complimentary metal oxide semiconductor (CMOS) devices.

(2) Description of Prior Art

To continually enhance semiconductor device performance sub- 90 nm metal oxide semiconductor field effect transistor (MOSFET) devices are now being fabricated. Advances in specific semiconductor fabrication disciplines such as photolithography and dry etching have allowed sub-90 nm MOSFET devices featuring narrow channel lengths to be routinely obtained. However in addition to breakthroughs in process disciplines sub- 90 nm devices are also being fabricated using materials such as high dielectric constant (high k) gate insulator layers as well as metal gate structures, which offer enhanced performance when compared to conventional counterparts such as silicon dioxide gate insulator layers and polysilicon gate structures. High k layers allow electrically thinner gate insulator layers to be employed with a reduced risk of leakage when compared to silicon dioxide gate insulator counterparts, while metal gate structures

help to reduce gate dielectric thickness by avoiding depletion effects present in polysilicon gates and offer decreased word line resistance when compared to more resistive polysilicon gate structures. To decrease word line resistance metal silicide regions are formed on the polysilicon gate structures, however this composite still does not reduce word line resistance to a level comparable to metal gate structures.

The use of metal gate structures can however add process complexity specifically when the metal gate structure is subjected to a salicide procedure which is used to form metal silicide on source/drain regions of a MOSFET or of a CMOS device. The salicide process results in the formation of metal silicide on source/drain regions after metal deposition and annealing procedures, while leaving unreacted metal on the surface of insulator layers such as sidewall insulator spacers located on the sides of the gate structure. Selective removal of unreacted metal via wet etch procedures can however result in unwanted removal or attack of an exposed metal gate structure, resulting in decreased word line resistance.

The present invention will teach a process sequence in which salicide processing is successfully coupled with metal gate structures, without degradation of the metal gate structure during wet etch procedures used to selectively remove unreacted metal from the surface of the sidewall insulator spacers. Prior art such as Besser et al in U.S. Pat. No. 6,436,840 B1, Besser et al in U.S. Pat. No. 6,440,868 B1, as well as Gardner et al in U.S. Pat. No. 6,326,251 B1, describe process sequences in which metal silicide is formed on MOSFET devices comprised with metal gate structures, however these prior art describe process

sequences more complex and costly than the simplified process offered in the present invention. In addition prior art such as Nguyen et al in U.S. Pat. No. 6,084,279, and Lin et al in U.S. Pat. No. 6,475,908 B1, describe MOSFET devices featuring metal gate structures however without integration of metal silicide regions. None of the above prior art however describe the unique process sequence offered in the present invention in which a salicide procedure is integrated with metal gate structures in a simplified process sequence and without damage to the metal gate structure during selective removal of unreacted metal.

SUMMARY OF THE INVENTION

It is an object of this invention to form a MOSFET or CMOS device featuring a metal gate structure on a high k gate insulator layer.

It is another object of this invention to form self -aligned metal silicide regions on both source/drain regions as well as on the top of the metal gate structure.

It is still another object of this invention to employ a thin amorphous silicon region on the top surface of the metal gate structure prior to the salicide procedure to provide a component for formation of a metal silicide shape on the metal gate structure, wherein the overlying metal silicide shape will then subsequently provide protection of the underlying metal gate structure during the wet etch selective removal of unreacted metal.

In accordance with the present invention a method of forming metal silicide regions for a

MOSFET device featuring a metal gate structure, is described. After formation of a high k gate insulator layer on a semiconductor substrate, a metal layer is deposited followed by the deposition of a thin amorphous silicon layer. Photolithographic and anisotropic dry etch procedures are used to form a metal gate structure with an overlying amorphous silicon shape, on the high k gate insulator layer. After formation of a lightly doped source/drain (LDD) region in an area of the semiconductor substrate not covered by the metal gate structure, composite insulator spacers are formed only on the sides of the metal gate structure and on the sides of the overlying amorphous silicon shape. After formation of a heavily doped region in an area of the semiconductor substrate not covered by the metal gate structure or by the composite insulator spacers, a blanket metal layer is deposited. An anneal procedure is next employed resulting in formation of metal silicide on the heavily doped source/drain region. The combination of metal on the exposed top surface of the amorphous silicon shape also results in formation of metal silicide on the metal gate structure, while portions of the metal layer located on the composite insulator spacers remain unreacted. Wet etch procedures are used to selectively remove the unreacted portions of metal from the surface of the composite insulator spacers, while metal silicide regions on both source/drain and on the top of the metal gate structure remain unetched, with the metal silicide located on the metal gate structure protecting the underlying metal gate structure during the selective removal procedure.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred

embodiments with reference to the attached drawings that include:

Figs. 1 - 8, which schematically in cross-sectional style show key stages used to fabricate a MOSFET device featuring a metal gate structure and employing a salicide procedure to form metal silicide regions on both source/drain as well as on the metal gate structure, and wherein the metal gate structure is protected during the salicide step used to selectively remove unreacted metal.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of fabricating a MOSFET device featuring a metal gate structure, and featuring a salicide process used to form metal silicide on a source/drain region as well as on the metal gate structure, and wherein the metal gate structure is protected from the salicide etch back step used to selectively remove unreacted metal, will now be described in detail. Although this invention will be described for an N channel, MOSFET device, it should be understood that this invention can also be applied to a P channel MOSFET device, or to a CMOS device comprised of both N channel and P channel MOSFET devices.

Semiconductor substrate 1, comprised of single crystalline P type silicon, featuring a <100> crystallographic orientation, is used and schematically shown in Fig. 1. Insulator layer 2a, featuring a high dielectric constant (high k), is next formed on semiconductor substrate 1. High k layer 2a, can be comprised of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide, hafnium aluminum oxide or a combination of oxides and

silicates of hafnium, zirconium etc,.featuring a dielectric constant greater than 4. High k layer 2a, shown schematically in Fig. 1, is formed at a thickness between about 15 to 150 Angstroms, via chemical vapor deposition (CVD) procedures. Conductive layer 3a, comprised of a refractory metal such as tungsten, molybdenum, tantalum, titanium, or comprised of a metal nitride material, is next formed on high k, gate insulator layer 2a, at a thickness between about 800 to 2000 Angstroms, via physical vapor deposition (PVD) procedures. A critical amorphous silicon layer 4a, is next formed on metal layer 3a, at a thickness between about 200 to 1000 Angstroms, via a low pressure chemical vapor deposition (LPCVD), or via a plasma enhanced chemical vapor deposition (PECVD) procedure. The thickness of amorphous silicon layer 4a, used to protect a subsequently defined metal gate structure from a wet etch procedure used to selectively remove unreacted metal during a salicide procedure, is adjusted to either be fully or partially consumed during the salicide procedure. Photoresist layer 5a, is next applied on amorphous silicon layer 4a. The result of the above procedures is schematically shown in Fig. 1.

Photolithographic exposure and development procedures are next employed to define photoresist shape 5b, at a width between about 0.05 to 2 micrometers. Using photoresist shape 5b, as an etch mask an anisotropic reactive ion etch (RIE) procedure defines metal gate structure 3b, on high k gate insulator layer 2a. The anisotropic RIE procedure, performed using Cl_2 as an etchant for conductive materials, also allows definition of amorphous silicon shape 4b, overlying metal structure 3b, to be accomplished. The anisotorpic RIE procedure selectively terminates at the appearance of high k gate insulator layer 2a. The result of these

procedures is schematically described in Fig. 2.

Removal of photoresist shape 5b, is accomplished via plasma oxygen ashing procedures and wet clean procedures. The wet clean procedures, performed using buffered hydrofluoric acid or dilute hydrofluoric acid as a component, allows removal of the portions of high k gate insulator layer 2a, not covered by metal gate structure 3b, to occur, resulting in only high k gate insulator 2b, now remaining underlying metal gate structure 3b. Lightly doped source/drain (LDD) region 6, is next formed in top portions of semiconductor substrate 1, not covered by the metal gate structure. This is accomplished via implantation of arsenic or phosphorous ions, at an energy between about 0.5 to 10 KeV, at a dose between about 5E14 to 2E15 atoms/cm^2. This is schematically shown in Fig. 3. If this invention is being applied to a P channel MOSFET device an N well region would be initially formed in a top portion of the semiconductor substrate and a P type LDD region would be formed in top portions of the N well region via implantation of boron or BF_2 ions.

Formation of composite insulator spacers on the sides of metal gate structure 3b, and on the sides of amorphous silicon shape 4b, is next addressed and schematically described in Fig. 4. A silicon oxide layer is first deposited at a thickness between about 50 to 250 Angstroms via LPCVD or PECVD procedures, followed by deposition of an overlying silicon nitride layer obtained at a thickness between about 300 to 1000 Angstroms, again via LPCVD or PECVD procedures. An anisotropic RIE procedure using Cl_2 or CF_4 as a selective etchant for silicon nitride and using CHF_3 as an etchant for silicon oxide, is employed to define the composite

insulator spacers comprised of silicon nitride spacers 8, and silicon oxide spacers 7. Encapsulation of metal gate structure 3b, in regards to the sidewall composite insulator spacers as well as overlying amorphous silicon shape 4b, has now been accomplished.

Heavily doped source/drain region 9, shown schematically in Fig. 5, is next formed via implantation of arsenic or phosphorous ions into a region of semiconductor substrate 1, not covered by metal gate structure 3b, or by the composite insulator spacers. Again for this description a heavily doped N type source/drain region obtained at an implant energy between about 30 to 100 KeV, at a dose between about 1E15 to 1E16 atoms/cm^2 is employed, however if a P channel MOSFET device is desired a P type heavily doped source/drain region, accomplished via implantation of boron or BF_2 ions would be used. Activation of the implanted ions located in both LDD region 6, and heavily doped source/drain region 9, is accomplished via a rapid thermal anneal (RTA) procedure, performed at a temperature between about 900 to 1100° C, for a time between about 0.1 to 5 sec., in an inert ambient.

After a pre-clean procedure, performed using dilute hydrofluoric acid, metal layer 10a, a layer such as titanium, cobalt, nickel, zirconium, or tantalum, is deposited via PVD procedures to a thickness between about 50 to 500 Angstroms. If desired metal layer 10a, can be comprised of nickel - platinum. This is schematically shown in Fig. 6.

An RTA procedure is next employed at a temperature between about 450 to 900° C, for a time between about 30 to 400 sec., in an inert ambient such as nitrogen or argon, resulting in formation of metal silicide regions 10b, on heavily doped source/drain region 9. The RTA

procedure also results in formation of metal silicide region 10c, located overlying metal gate structure 3b, accomplished via reaction of metal layer 10a, and a portion of amorphous silicon shape 4b. The thickness of amorphous silicon shape 4b, the thickness of metal layer 10a, as well RTA conditions, determine the extent of formation of metal silicide region 10c. If desired the above parameters can be designed to form metal silicide region 10c, on a non-consumed bottom portion of amorphous silicon shape 4b, or as shown schematically in Fig. 7, the above parameters, metal layer and amorphous silicon thickness as well as RTA conditions, can be designed to totally consume amorphous silicon shape 4b. Independent of the level of consumption of amorphous silicon shape 4b, the critical aspect is coverage or protection of the top surface of metal gate structure 3b, providing by metal silicide region 10c, during a subsequent wet etch procedure. Portions of metal layer 10a, located on the composite insulator spacers remain unreacted during the RTA procedure.

Removal of unreacted portions of metal layer 10a, is next addressed via a selective wet etch procedure, performed at a temperature between about 50 to 200° C, using a solution comprised of HCl - H_2O_2 - NH_4OH - H_2SO_4. The selective wet etch solution removes metal layer 10a, from the surface of the composite insulator spacers, while metal silicide region 10b, and metal silicide region 10c, are not attacked. If metal silicide region 10c, was not present metal gate structure 3b, would be attacked, eroded or damaged by the wet etch procedure. The presence

the amorphous silicon shape allowed formation of metal silicide region 10c, to be realized, in turn offering the protection needed by the metal gate structure during the wet etch procedure

employed to remove unreacted metal. The result of this procedure is schematically shown in Fig. 8. If desired another RTA procedure can be performed to lower the resistance of the metal silicide regions.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is: